CLAIMS

What is claimed is:

1. A circuit, comprising:

a first switch unit connectable to a first power line, a control line, and a bus line of an assisted Gunning transceiver logic (AGTL)-type bus, the first switch unit having an impedance that substantially matches the characteristic impedance of the bus line, wherein the first switch unit to electrically connect the first power line and the bus line when enabled by a control signal received via the control line; and

a second switch unit connectable to a second power line and the bus line, the second switch unit having an impedance different from that of the first switch unit, wherein the second switch unit to electrically connect a second power line and the bus line when enabled, the second switch unit to be disabled when the first switch unit is enabled and to be enabled when the first switch unit is disabled.

2. The circuit of claim 1, wherein the second switch unit's impedance is half that of the first switch unit.

3. The circuit of claim 1, further comprising an amplifier having an input terminal connected to the bus line.

4. The circuit of claim 1, wherein the first switch unit comprises a P-channel transistor.

5. The circuit of claim 4, wherein the first switch unit further comprises a resistor connected in series with the P-channel transistor.

6. The circuit of claim 4, wherein the resistor is a N-well resistor.

7. The circuit of claim 4, further comprising a trim circuit coupled to the P-channel transistor, wherein the trim circuit to compare the impedance of the first switch unit to a reference impedance and to adjust the impedance of the first switch unit to substantially match the reference impedance.

8. The circuit of claim 7, wherein the P-channel transistor comprises a plurality of component P-channel transistors, and wherein the trim circuit to adjust P-channel transistor's effective width-to-length ratio by selectively enabling one or more of the plurality of component P-channel transistors.

9. The circuit of claim 1, wherein the second switch unit comprises an N-channel transistor.

10. The circuit of claim 9, wherein the second switch unit further comprises a resistor connected in series with the N-channel transistor.

11. A circuit, comprising:

first means for electrically connecting to a first power line and a bus line of an assisted Gunning transceiver logic (AGTL)-type bus when enabled, the first means having an impedance that substantially matches the bus line's characteristic impedance; and

second means for electrically connecting a second power line and the bus line when enabled, the second means having an impedance different from that of the first means, wherein the second means is disabled when the first means is enabled and is enabled when the first means is disabled.

12. The circuit of claim 11, wherein the impedance of the second means is half that of the first means.

13. The circuit of claim 11, wherein the first means comprises a P-channel transistor and the second means comprises an N-channel transistor.

14. The circuit of claim 13, further comprising a trim circuit coupled to the P-channel transistor, wherein the trim circuit to compare the impedance of the first means to a reference impedance and to adjust the impedance of the first means to substantially match the reference impedance.

15. The circuit of claim 13, wherein the first means further comprises a resistor connected in series with the P-channel transistor.

16. A method, comprising:

causing a driver/receiver circuit to be in one of a plurality of modes that include a driver mode and a receiver mode, wherein the driver/receiver circuit is coupled to a bus line of an assisted Gunning transceiver logic (AGTL)-type bus, the driver/receiver circuit having a pull-up path and a pull-down path coupled to the bus line, the pull-up path having an impedance that substantially matches the bus line's characteristic impedance, the pull-down path having an impedance different from that of the pull-up path;

disabling the pull-down path and enabling the pull-up path when the driver/receiver circuit is in the receiver mode;

disabling the pull-down path and enabling the pull-up path when the driver/receiver circuit is in the driver mode to drive a logic high level on the bus line; and

disabling the pull-up path and enabling the pull-down path of when the driver/receiver circuit is in the driver mode to drive a logic low level on the bus line.

17. The method of claim 16, further comprising adjusting the impedance of the pull-up path to substantially match a reference impedance.

18. The method of claim 16, wherein the impedance of the pull-down path is about half that of the pull-up path.

19. The method of claim 16, wherein disabling the pull-down path comprises turning off an N-channel transistor having its source electrically connected to a ground bus and its drain coupled to the bus line.

20. The method of claim 19, wherein a resistor couples the drain of the N-channel transistor to the bus line.

21. A system, comprising:

an assisted Gunning transceiver logic (AGTL)-type bus;

a first driver/receiver circuit coupled to one end of a bus line of the AGTL-type bus, the first driver/receiver circuit including:

a first pull-up switch unit to couple a first power line to the bus line, wherein the first pull-up switch unit has an impedance substantially matching the bus line's characteristic impedance,

a first pull-down switch unit coupled to a first ground line and to the bus line, wherein the first pull-down switch unit has an impedance different from that of the first pull-up switch unit; and

a second driver/receiver circuit coupled to another end of the bus line, the second driver/receiver circuit including:

a second pull-up switch unit to electrically connect a second power line to the bus line, the first and second power lines having substantially identical voltage levels, wherein the second pull-up switch unit has an impedance substantially matching that of the first pull-up switch unit, and

a second pull-down switch unit coupled to a second ground line and to the bus line, the first and second ground lines having substantially identical voltage levels, wherein the second pull-down switch unit has an impedance substantially matching that of the first pull-down switch unit.

22. The system of claim 21, wherein the first pull-down switch unit's impedance is half that of the first pull-up switch unit.

23. The system of claim 21, wherein the first and second driver/receiver circuits each further comprise an amplifier having an input terminal connected to the bus line.

24. The system of claim 21, wherein the first pull-up switch unit comprises a P-channel transistor having one terminal coupled to the first power line.

25. The system of claim 24, wherein the first pull-up switch unit further comprises a resistor connected in series with the P-channel transistor's channel.

26. The system of claim 24, further comprising a trim circuit coupled to the P-channel transistor, wherein the trim circuit to compare the impedance of the first pull-up switch unit to a reference impedance and to adjust the impedance of the first pull-up switch unit to substantially match that of the reference impedance.

27. The system of claim 26, wherein the P-channel transistor comprises a plurality of component P-channel transistors, and wherein the trim circuit to adjust P-channel transistor's effective width-to-length ratio by selectively enabling one or more of the plurality of component P-channel transistors.

28. The system of claim 21, wherein the first pull-down switch unit comprises an N-channel transistor.